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Atty. Dkt. No. 039153-0457 (G1162)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicants: Lopatin et al.

Title: METHOD OF USING TERNARY COPPER ALLOY TO OBTAIN A LOW RESISTANCE AND LARGE GRAIN SIZE INTERCONNECT

Appl. No.: 09/994,395

Filing Date: 11/26/2001

Examiner: Ori Nadav

Art Unit: 2811

Confirmation Number: 7882

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Examiner Nadav:

Under the provisions of 37 C.F.R. § 41.37, this Appeal Brief is being filed together with a check in the amount of $500.00 covering the 37 C.F.R. § 41.20(b)(2) appeal fee. If this fee is deemed to be insufficient, authorization is hereby given to charge any deficiency (or credit any balance) to the undersigned deposit account 50-2350.

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1. REAL PARTY IN INTEREST

The real party in interest is the assignee of record, Advanced Micro Devices, Inc. (as recorded in the records of the United States Patent and Trademark Office at Reel/Frame 012331/0426 on November 26, 2001).

2. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences that will directly affect, be directly affected by, or have a bearing on the present appeal, that are known to Appellants or Appellants' patent representative.

3. STATUS OF CLAIMS

The present appeal is directed to Claims 1-4, 6, 8-13, 15-20, 22, and 23, all of which stand rejected pursuant to a final Office Action dated June 26, 2006.

4. STATUS OF AMENDMENTS

Claims 1-4, 6, 8-13, 15-20, 22, and 23 were pending in the application when a final Office Action dated June 26, 2006, was issued. An Advisory Action was issued on August 21, 2006. A Notice of Appeal was filed August 30, 2006.

5. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates generally to the fabrication of integrated circuits. See present application, page 1, paragraph [0002] and Figure 4. An exemplary embodiment includes a method forming a barrier layer along lateral side walls and a bottom of a via aperture and providing a ternary copper alloy via material in the via aperture to form a via. (See Para [0014].) The ternary copper alloy via material includes at least one element for increasing the grain size. (See Para [0032].)

Independent Claim 1 relates to a method of fabricating an integrated circuit. The method includes depositing an etch stop layer (e.g., etch stop layer 474, FIG. 4) over a first conductive

layer (e.g., conductive layer 430, FIG. 4), where the etch stop layer is in direct contact with the first conductive layer. The method further includes depositing an insulating layer (e.g., dielectric layer 442, FIG. 4) after the etch stop layer is deposited over the etch stop layer, forming a barrier layer (e.g., barrier layer 440, FIG. 4) extending along lateral side walls and a bottom of a via aperture (e.g., via section 420, FIG. 4), and depositing a copper alloy via material in the via aperture to form a via. The via aperture is configured to receive a via material that electrically connects a first conductive layer and a second conductive layer. The copper alloy material includes zinc (Zn) or silver (Ag) and at least one element increasing grain size including calcium (Ca) or chromium (Cr). (See Para. [0032]-[0033].)

Independent claim 10 relates to a method of using ternary copper alloy to obtain a low resistance and large grain size interconnect or via. The method includes providing a first conductive layer (e.g., conductive layer 430, FIG. 4) or an integrated circuit substrate, providing an etch stop layer (e.g., etch stop layer 474, FIG. 4) over the first conductive layer where the etch stop layer is in direct contact with the first conductive layer providing an insulating layer (e.g., dielectric layer 442, FIG. 4). After the etch stop layer has been provided over the first conductive layer, providing a conformal layer section (e.g., barrier layer 440, FIG. 4) extending along a bottom and sides of a via aperture (e.g., via section 420, FIG. 4), positioned over the first conductive layer to form a barrier separating the via aperture from the first conductive layer, filling the via aperture with a ternary copper alloy via material to form a ternary copper alloy via, and providing a second conductive layer (e.g., conductive via layer 410, FIG. 4) over the ternary copper alloy via such that the ternary copper alloy via electrically connects the first conductive layer to the second conductive layer. The ternary copper alloy includes at least one element for increasing grain size and at least one of chromium (Cr) or calcium (Ca) where the ternary copper alloy material includes an element with a characteristic for increasing grain size of the ternary copper alloy via. (See Para. [0032].)

Independent claim 17 relates to a method of forming a via in an integrated circuit. The method includes depositing a first conductive layer (e.g., conductive layer 630, FIG. 6),

depositing an etch stop layer (e.g., etch stop layer 674, FIG. 6) over the first conductive layer, where the etch stop layer is in direct contact with the first conductive layer, depositing an insulating layer (e.g., dielectric layer 642, FIG. 6) over the etch stop layer, forming an aperture in the insulating layer and the etch stop layer, providing a barrier material extending along a bottom and sides of the aperture to form a barrier layer (e.g., barrier layer 640, FIG. 6), filling the aperture with a ternary copper alloy via material to form a ternary copper alloy via, (e.g., via/trench Section 620, FIG. 6), and providing a second conductive layer (e.g., conductive layer 610, FIG. 6) over the ternary copper alloy via such that the ternary copper alloy via electric connects the first conductive layer and the second conductive layer. (See Para. [0042].) The ternary copper alloy via includes at least one of the following pairs of elements, Tin and Calcium, Tin and Chromium, Zinc and Chromium, Zinc and Calcium, Silver and Chromium, and Silver and Calcium. The ternary copper alloy via material includes an element with a characteristic for increasing grain size of ternary copper alloy via.

6. GROUND OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection that Appellants request the Board review are provided below. Appellants respectfully submit that the Examiner erred in rejecting:

1. Claims 1-3, 6-8, 10, 13, and 15-20 as being unpatentable under 35 U.S.C. § 103(a) over U.S. Patent No. 6,482,740 (Soininen et al.) in view of U.S. Patent No. 6,399,496 (Edelstein et al.) and U.S. Patent 6,749,689 (Bögel et al.).

2. Claims 4 and 22 as being unpatentable under 35 U.S.C. § 103(a) over Soininen et al., Edelstein et al., and Bögel et al. and further in view of U.S. Patent No. 6,440,849 (Merchant et al.).

3. Claims 9 and 23 as being unpatentable under 35 U.S.C. § 103(a) over Soininen et al., Edelstein et al., and Bögel et al. and further in view of U.S. Patent No. 6,380,083 (Gross).

4. Claims 11-12 as being unpatentable under 35 U.S.C. § 103(a) over Soininen et al., Edelstein et al., and Bögel et al., and further in view of U.S. Patent No. 6,090,710 (Andricacos et al.).

7. ARGUMENT

A. LEGAL STANDARDS

Claims 1-4, 6, 8-13, 15-20, 22, and 23 have been rejected under 35 U.S.C. § 103(a), which states:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The legal standards under 35 U.S.C. § 103(a) are well-settled. Obviousness under 35 U.S.C. § 103(a) involves four factual inquiries: 1) the scope and content of the prior art; 2) the differences between the claims and the prior art; 3) the level of ordinary skill in the pertinent art; and 4) secondary considerations, if any, of nonobviousness. See Graham v. John Deere Co., 383 U.S. 1, 148 U.S.P.Q. 459 (1966).

In proceedings before the Patent and Trademark Office, the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art. In re Piasecki, 745 F.2d 1468, 1471-72, 223 U.S.P.Q. 785, 787-88 (Fed. Cir. 1984). "'[The Examiner] can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references.'" In re Fritch, 972 F.2d 1260, 1265, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992).

As noted by the Federal Circuit, the "factual inquiry whether to combine references must be thorough and searching." McGinley v. Franklin Sports, Inc., 262 F.3d 1339, 60 USPQ.2d 1001 (Fed. Cir. 2001). Further, it "must be based on objective evidence of record." In re Lee, 277 F.3d 1338, 61 USPQ.2d 1430 (Fed. Cir. 2002). The teaching or suggestion to make the claimed combination must be found in the prior art, and not in the applicant's disclosure. In re

Vaeck, 947 F.2d 488, 20 USPQ.2d 1438 (Fed. Cir. 1991). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ.2d 1430 (Fed. Cir. 1990). "It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to '[use] that which the inventor taught against its teacher.'" Lee (citing W.L. Gore v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983)).

B. REJECTIONS OF CLAIMS 1-4, 6, 8-13, 15-20, 22, AND 23 UNDER 35 U.S.C. § 103(a) BASED ON SOININEN ET AL. IN VIEW OF EDELSTEIN ET AL., BÖGEL ET AL. AND VARIOUS OTHER REFERENCES

In the final Office Action dated June 26, 2006, Claims 1-4, 6, 8-13, 15-20, 22, and 23 were rejected under 35 U.S.C. § 103(a) over Soininen et al. in view of Edelstein et al., Bögel et al. and other various references. The Examiner maintained these rejections in the Advisory Action mailed August 21, 2006. Appellants respectfully request the Board reverse the rejections maintained by the Examiner for at least the reasons that are described below.

I. The Examiner's rejection of Claims 1-3, 6-8, 10, 13, and 15-20 under 35 U.S.C. § 103(a) over Soininen et al. in view of Edelstein et al. and Bögel et al. should be reversed because at least one limitation of each of these claims is not taught or suggested by the combination.

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art (see M.P.E.P. § 2143.03). The rejected claims would not have been obvious to one of ordinary skill in the art at the time of the invention because at least one limitation from independent Claims 1, 10, and 17 is not taught or suggested by the combination of Soininen et al. in view of Edelstein et al. and Bögel et al..

For example, independent Claim 1 requires:

> the copper alloy material including Zinc (Zn) or Silver (Ag) and at least one element for increasing grain size including Calcium (Ca) or Chromium (Cr).

In the Office Action mailed January 11, 2006, the Examiner admits that "*Soininen et al. do not teach the copper alloy material including Zinc (Zn) or Silver (Ag) and at least one element for increasing grain size including Calcium (Ca) or Chromium (Cr).*" (Page 3.) In the Office Action, Examiner relies on Edelstein et al. and Bögel et al. as providing the missing teaching. However, Appellants' response points out that Edelstein et al. does not mention grain size ***at all***. Edelstein et al. describes the use of "seed layers." The section referred to by the Examiner in the Office Action – Col. 8, lines 35-52 – states that seed layers are used to "improve the adhesion properties relative to pure copper." (Col. 8, lines 36-37.) Bögel et al. does not provide the missing teaching either. It describes change in grain growth due to *annealing time* and *temperature*, not by the addition of an element.

In the Final Office Action mailed June 26, 2006, the Examiner admits "***Edelstein et al. and Bögel et al. do not explicitly state increasing the grain size due to chromium.***" (Page 6, emphasis added.) Yet the rejections based on Edelstein et al. and Bögel et al. are maintained because the Examiner alleges that "*increasing the grain size due to chromium*" is "*inherent in prior art's devices, because the addition of Calcium (Ca) or Chromium (Cr) increases grain size.*" Appellants' response to the Final Office Action requests the Examiner provide evidence to support the assertion of inherency, as required by M.P.E.P. 2112. The Examiner gives no such evidence or basis in fact. Rather, in the Advisory Action dated August 21, 2006, the Examiner states:

> The Examiner maintains the position that the addition of calcium (Ca) or chromium (Cr) increases grain size, because Applicant clearly states that the addition of calcium (Ca) or chromium (Cr) increases grain size. Note that the combination do not rely on hindsight because the combination is based on providing the device stable Cu alloy with improved electromigration properties.

(Advisory Action, page 3, emphasis added.)

The Examiner's comment does not seem to make logical sense. It appears that the Examiner is arguing that adding calcium (Ca) or chromium (Cr) increases grain size because the

Appellants say so! The Examiner's comments in the Advisory Action are not responsive and provide no support for the underlying rational for the rejection. Moreover, the Examiner is using improper "hindsight" using Appellants' teachings for the rejection. The Examiner suggests that he is not using hindsight because "*the combination is based on providing the device stable Cu alloy with improved electromigration properties.*" Nevertheless, whether or not the combination of the references provides improved electromigration properties has nothing to do with using an element, such as Ca or Cr, to increase grain size!

As the Examiner has admitted, none of the cited references teach or suggest:

> "depositing a copper alloy material...including...at least one element for increasing grain size including Calcium (Ca) or Chromium (Cr),"

required by Claim 1, or

> "the ternary copper alloy via material includes an element with a characteristic for increasing grain size of the ternary copper alloy via,"

required by independent Claims 10 and 17. Moreover, there is no evidence to support the Examiner's new position that these teachings are "inherent."

The rejection of Claims 1-3, 6-8, 10, 13, and 15-20 under 35 U.S.C § 103(a) should be withdrawn. The combination of Soininen et al., Edelstein et al., and Bögel et al. proffered by the Examiner fails to suggest or teach at least one limitation of each of these rejected claims. As such, the Board should find that the Examiner has not established a prima facie case of obviousness and reverse the rejection.

II. The Examiner's rejection of dependent Claims 4, 9, 11-12, 22 and 23 should be reversed because at least one limitation of each of these claims is not taught or suggested by the combinations offered by the Examiner.

Claims 4 and 9 depend from independent Claim 1 and, as such, include all of the limitations of Claim 1. As explained above with respect to independent Claim 1, the

combination of Soininen et al., Edelstein et al., and Bögel et al. fail to suggest or teach "depositing a copper alloy material...including...at least one element for increasing grain size including Calcium (Ca) or Chromium (Cr)," required by Claim 1. In rejecting Claim 4, Examiner points to Merchant et al., but Merchant et al. does not suggest or teach increasing grain size using Calcium (Ca) or Chromium (Cr). In rejecting Claim 9, the Examiner points to Gross, but Gross also does not suggest or teach increasing grain size using Calcium (Ca) or Chromium (Cr).

Claims 22 and 23 depends from independent Claim 17 and, as such, include all of the limitations of Claim 17. As explained above, the combination of Soininen et al., Edelstein et al., and Bögel et al. fail to suggest or teach "the ternary copper alloy via material includes an element with a characteristic for increasing grain size of the ternary copper alloy via," required by independent Claim 17. In the rejection of Claim 22, Examiner points to Merchant et al., but Merchant et al. does not suggest or teach an element with a characteristic for increasing grain size of the ternary copper alloy via. In the rejection of Claim 23, Examiner points to Gross, but Gross does not suggest or teach an element with a characteristic for increasing grain size of the ternary copper alloy via.

Claims 11 and 12 depend from independent Claim 10 and, as such, include all of the limitations of Claim 10. As explained above, the combination of Soininen et al., Edelstein et al., and Bögel et al. fail to suggest or teach "the ternary copper alloy via material includes an element with a characteristic for increasing grain size of the ternary copper alloy via," required by independent Claim 10. In rejecting Claim 11-12, the Examiner points to Andricacos et al., but Andricacos et al. does not provide this missing teaching.

The rejection of dependent Claims 4, 9, 11-12, 22 and 23 should be withdrawn because the combinations cited by the Examiner fail to suggest or teach at least one limitation of each of these claims.

III. The Examiner's rejection of the pending claims should be reversed because there is no suggestion or motivation to combine the teachings of the references cited by the Examiner.

To establish a prima facie case of obviousness based on a combination of prior art references under 35 U.S.C. § 103(a), the Examiner must first show that there is a suggestion or motivation to combine the teachings of those references. This may come in the form of some objective teaching in the prior art or, alternatively, knowledge generally available to one of ordinary skill in the art at the time of the invention that would lead that individual to combine the relevant teachings of the references. When the motivation to combine the teachings of the references is not immediately apparent, it is the duty of the Examiner to explain why the combination of the teachings is proper. Ex parte Skinner, 2 U.S.P.Q.2d 1788 (Bd. Pat. App. & Inter. 1986).

In the present case, the rejections are based, at least in part, on the combination of Soininen et al., Edelstein et al., and Bögel et al.. The Examiner refers to Bögel et al. because, according to the Examiner, Soininen et al. does not teach increasing grain size using Calcium (Ca) or Chromium (Cr). As discussed above, Appellants contend that Bögel et al. does not provide this teaching. Assuming *arguendo* that it does, a person of skill in the art would not look to Bögel et al. for the teachings missing in Soininen et al. Bögel et al. specifically states that its invention is directed to "under the hood automotive applications" (Col. 4, lines 60-61). There is no suggestion that such a reference would be combined with Soininen et al., which relates to the "manufacturing of integrated circuits" (Abstract). Bögel et al. is not within the Appellants' field of endeavor and, further, Bögel et al. does not relate to a particular problem addressed by Appellants' claimed invention, namely increasing electromigration properties by increasing the grain size in a via material. (See M.P.E.P. 2141.01(a).) The Board should find that there is no suggestion or motivation to combine Bögel et al. with Soininen et al., as the Examiner did in rejecting Claims 1-4, 6, 8-13, 15-20, 22, and 23.

8. CONCLUSION

In view of the foregoing, Appellants submit that Claims 1-4, 6, 8-13, 15-20, 22, and 23 are not properly rejected under 35 U.S.C. § 103(a) and are, therefore, patentable. Accordingly, the Appellants respectfully request that the Board reverse all claim rejections and indicate that a notice of allowance respecting all pending claims should be issued.

Respectfully submitted,

Date October 3, 2006

By _____

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Paul S. Hunter
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CLAIMS APPENDIX

1. (Previously Presented) A method of fabricating an integrated circuit, the method comprising:

depositing an etch stop layer over a first conductive layer, wherein the etch stop layer is in direct contact with the first conductive layer;

depositing an insulating layer after the etch stop layer is deposited over the etch stop layer;

forming a barrier layer extending along lateral side walls and a bottom of a via aperture, the via aperture being configured to receive a via material that electrically connects the first conductive layer and a second conductive layer; and

depositing a copper alloy via material in the via aperture to form a via, the copper alloy material including Zinc (Zn) or Silver (Ag) and at least one element for increasing grain size including Calcium (Ca) or Chromium (Cr).

2. (Previously Presented) The method of claim 1, wherein the copper alloy via material includes silver (Ag).

3. (Previously Presented) The method of claim 2, wherein the copper alloy via material includes Zinc (Zn).

4. (Previously Presented) The method of claim 1, wherein the copper alloy via material includes one atomic percent or less of Zinc (Zn) or Silver (Ag).

5. (Cancelled)

6. (Previously Presented) The method of claim 1, wherein the copper alloy via material includes Chromium (Cr).

7. (Cancelled)

8. (Previously Presented) The method of claim 6, wherein the element with a characteristic for increasing grain size is one atomic percent or less of Chromium (Cr).

9. (Original) The method of claim 6, wherein the increased grain size is between 0.5 and 3 μm.

10. (Previously Presented) A method of using ternary copper alloy to obtain a low resistance and large grain size interconnect or via, the method comprising:

providing a first conductive layer over an integrated circuit substrate;

providing an etch stop layer over the first conductive layer, wherein the etch stop layer is in direct contact with the first conductive layer;

providing an insulating layer over the etch stop layer after the etch stop layer has been provided over the first conductive layer;

providing a conformal layer section extending along a bottom and sides of a via aperture positioned over the first conductive layer to form a barrier separating the via aperture from the first conductive layer;

filling the via aperture with a ternary copper alloy via material to form a ternary copper alloy via, the ternary copper alloy including at least one element for lowering resistivity and at least one of Chromium (Cr) or Calcium (Ca), wherein the ternary copper alloy via material includes an element with a characteristic for increasing grain size of the ternary copper alloy via; and

providing a second conductive layer over the ternary copper alloy via such that the ternary copper alloy via electrically connects the first conductive layer to the second conductive layer.

11. (Previously Presented) The method of claim 10, wherein the ternary copper alloy via material is at least 98 atomic percent copper.

12. (Previously Presented) The method of claim 11, wherein the ternary copper alloy via includes Zinc (Zn), Silver (Ag), or Tin (Sn).

13. (Previously Presented) The method of claim 11, wherein the ternary copper alloy via includes one atomic percent or less of Chromium (Cr) or Calcium (Ca).

14. (Cancelled)

15. (Previously Presented) The method of claim 10, wherein the element with a characteristic for increasing grain size is Calcium (Ca) or Chromium (Cr).

16. (Previously Presented) The method of claim 10, wherein the element with a characteristic for increasing grain size is one atomic percent or less of the ternary copper alloy via material.

17. (Previously Presented) A method of forming a via in an integrated circuit, the method comprising:

depositing a first conductive layer;

depositing an etch stop layer over the first conductive layer, wherein the etch stop layer is in direct contact with the first conductive layer;

depositing an insulating layer over the etch stop layer;

forming an aperture in the insulating layer and the etch stop layer;

providing a barrier material extending along a bottom and sides of the aperture to form a barrier layer;

filling the aperture with a ternary copper alloy via material to form a ternary copper alloy via including at least one of the following pairs of elements: Tin and Calcium; Tin and Chromium; Zinc and Chromium; Zinc and Calcium; Silver and Chromium; and Silver and Calcium, wherein the ternary copper alloy via material includes an element with a characteristic for increasing grain size of the ternary copper alloy via; and

providing a second conductive layer over the ternary copper alloy via such that the ternary copper alloy via electrically connects the first conductive layer and the second conductive layer.

18. (Previously Presented) The method of claim 17, wherein the ternary copper alloy via material includes copper (Cu), tin (Sn), and Calcium (Ca).

19. (Original) The method of claim 17, wherein the ternary copper alloy via material includes copper (Cu), zinc (Zn), and chromium (Cr).

20. (Previously Presented) The method of claim 17, wherein the ternary copper alloy is CuAgCr, or CuSnCa.

21. (Cancelled)

22. (Previously Presented) The method of claim 17, wherein the ternary copper alloy via includes stuffed grain boundaries.

23. (Original) The method of claim 17, wherein the grain size of the ternary copper alloy via is 0.5 to 3 μm.

EVIDENCE APPENDIX

No evidence entered with this Brief.

RELATED PROCEEDINGS APPENDIX

There are no related appeals and interferences.

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